

Agilent ASUR Single Device Reliability

A Component of the Solution Suite
for Advanced Reliability



- Single-site device reliability
- Worldwide standard JEDEC compliant PDQ-WLR® library
- Support for BASIC and C language algorithms
- Graphical programless algorithms (IMT)
- SPECS test plans import/export
- SPECS algorithms compatibility
- Interactive to automated measurements
- Semi and auto 200 & 300 mm probe control

Nanometer era reliability system

ASUR SDR (C1281A) is a modular and scalable high-performance accelerated reliability test system for single-site studies using instrument-based solutions that incorporates the proven accelerated techniques of the worldwide standard PDQ-WLR.

ASUR SDR is the complete hardware and software solution which provides the flexibility to standardize and expand test cells and methodologies with different instruments through the built-in JEDEC PDQ-WLR library and custom algorithms capability. It is mission ready; same testing capabilities and structure, and added flexibility, as the industry standard system tester 4070 PDQ-WLR.

ASUR SDR provides users with an Interactive Measurement Tool (IMT) that allows quickly developing and testing custom algorithms without programming and compiling.

ASUR SDR can provide immediate feedback on device behavior through the use of its real-time plotting tool. In addition, sophisticated analysis of results is nearly instantaneous through the optional suite's Reliability Data Analyzer, ASUR RDA.

The ASUR SDR prober server supports from manual test to 200 and 300 mm semi and auto wafer prober environments.

ASUR SDR — The nanometer era solution

New materials and structures, advanced fabrication nodes and their processes create new chip reliability exposure for existing and emergent device technology which demands extraordinary amounts of reliability data. Detection, testing, modeling, simulation and control of *known* and *new* failure mechanisms determine the successful integration of new processes, materials, devices and their performance in modern circuit applications

Reliability tests for current and newer technologies such as those for 32 nm and beyond, are no longer exclusive to the DC domain; AC reliability and other significant statistical data is vital thus requiring tools to be extensible into emerging paradigms. ASUR SDR improves over preceding PDQ-WLR generations and includes algorithms in new domains required for advanced technology development and assessment.

Current ASUR SDR methods, including on-the-fly techniques down to 60 microseconds, are provided for DC and AC reliability testing of: gate oxides, bias-temperature instability (BTI), hot-carrier injection (HCI), electromigration, etc. Development and execution of SDR custom user algorithms is supported via the programless IMT component, or by more traditional methods using its advanced editors for BASIC, or C languages. Optional test code generation from IMT objects to BASIC or C source code is accomplished simply by the push-of-a-button.

All user interfaces in ASUR SDR are designed with the SPECS user in mind. The same test plan hierarchy is available and optimized for the instrument environment, and test plans can be directly imported or exported from system testers. The ASUR SDR application program interface follows the standard system TIS for direct use of SPECS BASIC or C algorithms. The algorithm builders simplify the creation and modification of algorithms.

The ASUR SDR architecture supports Kelvin, Pseudo-Kelvin and non-Kelvin wiring configurations for different operating conditions of devices, test techniques, instrumentation, etc. This flexibility in the topology permits users to scale their actual hardware test solutions and eliminate or reduce measurement variations and inaccuracies caused by residual parasitic components.

The nanometer era industry dilemma

Innovation has higher risk

Worldwide technology development centers and manufacturing sites require reliability measurement solutions that are highly modular and scalable as technology evolves and new paradigms are encountered. New and correct test solutions become the barrier between accurate reliability data and incorrect lifetime predictions: Technology success or failure

Extensive and diverse reliability tests are now necessary to meet new significant data metrics introduced by the ever evolving technological needs. The future is data driven, and meaningful data can only be attained by the expert integration of a test cell: equipment, software and test techniques for correct reliability assessment.

Solution suite for the nanometer

The development of nanometer scale technologies and new materials has brought testing challenges into the mainstream. Technological projections, their road maps and analysts' reports concur that modern reliability testing's impact on the semiconductor industry is enormous for the nanometer era. Reliability data is indispensable in the process of selecting new materials; therefore, it is critical to have modular scalable and cost-effective reliability testing for modern manufacturing.

Successful manufacturing of current technology depends uniquely on accurate reliability data and becomes even more so for deep nanometer scale.

Advanced Scalable Unified Reliability (ASUR)

Reliability data correlation with confidence from one instrument to systems

- ASUR provides reliability solutions from single- (SDR) to multi-site parallel (PDR) test
- Modular precision architecture and scalable test cell control
- PDQ-WLR Technology DNA in its sixth generation
- Superior phenomena detection beyond traditional methods now include DSP
- Reliability Data Analyzer (RDA) the only dedicated reliability analysis environment in the industry

ASUR is used in IDM, foundries, fabless and equipment companies, reducing development cycle time while helping control maturing processes through identification and prediction of reliability problems at all phases of the IC life cycle — development, qualification, production. ASUR Single Device Reliability (SDR) with multi-device test provides effortless expansion in capacity, new test needs and test cell standardization across multiple instruments, while growth is assured by the test cell scalability and modularity.

Agilent PDQ-WLR — reliability technology evolution

The ASUR SDR software suite provides an environment in which users can test semiconductor wafers by using the JEDEC compliant PDQ-WLR algorithm library. PDQ-WLR, now in its sixth generation, is a Predictive, Demonstrated and Quantitative methodology used in Production, Development and Qualification testing of semiconductor manufacturing processes. The easy-to-use ASUR SDR software suite comes equipped with PDQ-WLR and added features necessary for the reliability assessment of advanced technological nodes.

ASUR SDR supports user creation and modification of BASIC and C algorithms through standard editors or via the IMT programless environment. Optionally, users can add to SDR the Reliability Data Analyzer (RDA), a comprehensive reliability data analysis tool, and PDQ-Fab for test structure design.

ASUR SDR with its JEDEC compliant PDQ-WLR excels in uniquely providing the semiconductor industry with a proven solution and solid experience of over 13 years of demonstrated reliability solutions. This considerable expertise makes SDR the most sought after and trusted solution for reliability studies. The recognized success of PDQ-WLR makes SDR the ideal vehicle to ensure success for current and future deep nanometer technology.

ASUR SDR — at a glance

ASUR is the total integration of advanced modular scalable software, nanometer PDQ-WLR Library, and both standard and specialized hardware based on Agilent's reliability IP, real-life device test knowledge and unmatched test expertise.

ASUR SDR software features

- Ability to modify existing test algorithms and add new and custom test algorithms
- Use of output results from an algorithm as input values for a downstream algorithm
- Global variables and shell functions as used in Agilent Technologies SPECS test shell

- DSP phenomena detection
- HCI Builder, as used in Agilent PDQ-WLR, to make complex hot carrier test definitions fast and easy
- BTI Builder to select the best parameters and minimize any relaxation effects
- IMT (OO), HT BASIC and C scripting languages so no compilation necessary
- Flexible operation modes that range from programless interactive execution (IMT), to individual algorithm execution (algorithm mode) and to fully automatic test plan execution (test plan mode)
- Algorithm mode to access prober, tester, and test algorithm libraries (built-in and user defined, translation layer, etc.)
- Manual, semi and auto 200 and 300 mm wafer probers

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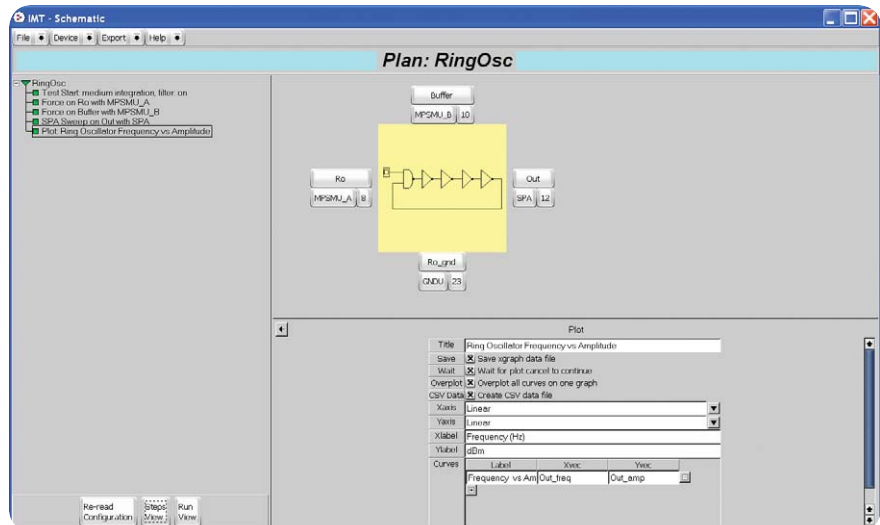
----- Body of Algorithma -----
Gpib_address=15
CardA=0
CardB=0
CardC=0
IF (2 MOD Mpsau=0) THEN GOTO Par_error
IF (2 MOD Mpsau=0) THEN GOTO Par_error
IF (2 MOD Mpsaub=0) THEN GOTO Par_error

IF (Forceconrolpin>36) THEN CardA=2
IF (Senseconrolpin>36) THEN
  CardB=2
ELSE
  IF (Mpsau=24) THEN CardB=1
END IF
Gpib_write("CARD_CONTROL", Gpib_address, "MAK:ROUT("&CardA_Input&","&CardA_Output&")")
Gpib_write("CARD_CONTROL", Gpib_address, "MAK:ROUT("&CardB_Input&","&CardB_Output&")")
IF (Low_noise_terminal>36) THEN
  CardC=2
ELSE
  IF (Forceconrolpin>24) THEN CardC=1
END IF
IF (Senseconrolpin<10) THEN
  Forceconrolpin$=VAL$(CardA)&"010"&VAL$(CardA_Input)
ELSE
  Forceconrolpin$=VAL$(CardA)&"01"&VAL$(CardA_Input)
END IF
Gpib_write("CARD_CONTROL", Gpib_address, "MAK:ROUT("&CardB_Input&","&CardB_Output&")")
Gpib_write("CARD_CONTROL", Gpib_address, "MAK:ROUT("&CardC_Input&","&CardC_Output&")")
END IF
ELSE
  IF (CardA_Input>24) THEN
    CardA=1
  END IF
Gpib_write("CARD_CONTROL", Gpib_address, "OUTPUT.OFF")
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User-programmable test algorithms

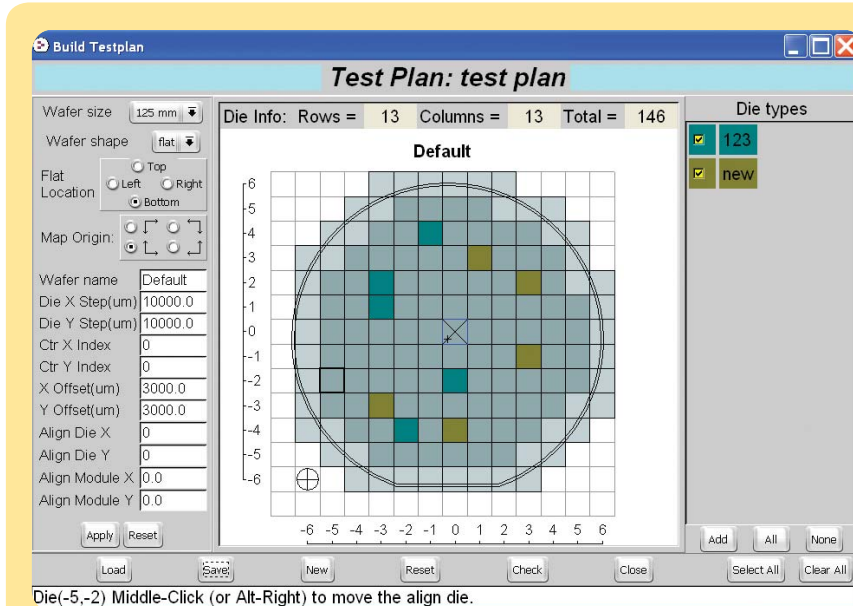
User-definable algorithms in C or BASIC language provide the ability to implement proprietary testing or customize testing for a unique device technology such as NVM HCI.

BASIC and C language support



Interactive measurement tool (IMT)

IMT has several important functions including direct bench-like control of the complete test cell. It also serves as a programless algorithm development tool that permits the interactive setups be used as objects in a test plan. The IMT created test objects can also be exported to BASIC or C source code for direct use as traditional algorithms in automated test plans.



ASUR SDR test plan execution

Reliability test with confidence

JEDEC standard reliability test algorithms in ASUR are in their fifth generation. This suite is fully tested and supported with over 10 years of in-field experience and validation.

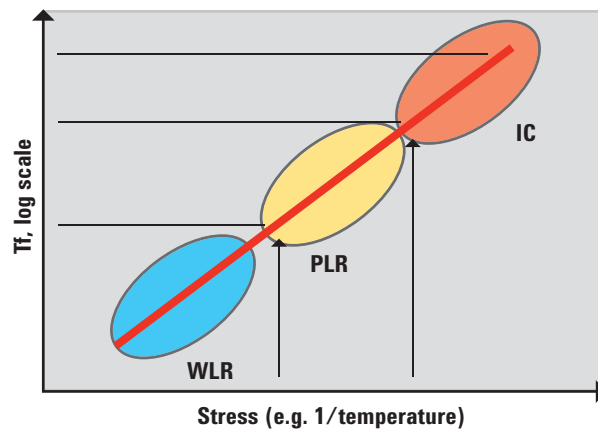
- Electromigration (EM)
- Bias temperature stress (BTS)
- Gate oxide integrity (GOI)
- Hot carrier injection (HCI)
- Bias temperature instability (BTI)

Use the ASUR RDA data analysis tools and the PDQ-Fab™ test structure library to define and end-to end reliability test strategy.

Nanometer PDQ-WLR library

ASUR SDR provides the semiconductor industry with reliability tests for deep nanometer technology development. The single-site industry standard JEDEC compliant PDQ-WLR library in its sixth generation includes:

- Current and voltage time dependent dielectric breakdown with stress induced leakage current (SILC) (JTDDDB and VTDDDB)
- Voltage ramp (VRAMP)
- Bias temperature stress (BTS)
- Gate oxide injection (GOI)
- Hot carrier injection (HCI)
- N and P bias temperature instability (NBTI and PBTI)
- Electromigration (EM)
- AC VTDDDB
- AC BTI
- AC HCI single and double pulse



Use condition (10 years)

ASUR SDR hardware features

Agilent ASUR SDR supports a vast range of instruments for solutions required in modern reliability. Those test cell components give various degrees of flexibility depending on the application sought and include

Standard

- Agilent 4155 | 6 B | C
- Agilent E5260A, E5270B, B1500A
- Agilent E5250, B2200, B2201 and third party switching matrices
- Agilent 81110A, 8114A pulse generators
- Agilent B1520A MFCMU, 4284A and E4080A CV meters
- Agilent 4294A impedance analyzer
- Agilent E5288A ASU, atto sense unit
- Agilent 41000-100 to -400 series systems
- Agilent power supplies, oscilloscopes, spectrum analyzers, frequency counters, etc.
- Agilent proprietary pseudo-Kelvin (Triax 2-to-1) Adapter C1280-61001



Agilent B1500A



Agilent B2201A

Specialized

In addition to the standard instruments, Agilent provides specialized reliability components such as the pseudo Kelvin adapter, shown below, to meet advanced needs.



Pseudo Kelvin adapter (C1280-61001)

Pseudomorphic Kelvin and full Kelvin wiring

Pseudomorphic Kelvin provides Kelvin-like compensated measurements with fewer switch matrix and cabling requirements. ASUR SDR and PDR support both traditional full-Kelvin and pseudomorphic Kelvin wiring topologies automatically.

Windows® system controller

Recommended computer	HP xw8400 Workstation
Operating system	Windows XP® Professional SP2 HT BASIC (8.5-9.1) C
Required memory	1 GB
Required disk	4 GB executable 250 GB minimum data

System software

Standard ASUR SDR software configuration

Provides the following capabilities:

- ASUR system core
- Interactive measurement tool (IMT)
- Test algorithm code auto generation to BASIC and C
- Automatic SPECS algorithms and test Plans import/export to/from ASUR SDR
- Off-line debugging
- JEDEC PDQ-WLR
- Real-time plot, Xgraph
- Interactive, algorithm and test plan control
- OS shell control commands
- OS remote X display supported
- Automatic data formatting data output
- TIS control library (standardized)
- Manual, semi and auto prober server for 200 mm and 300 mm

Agilent ASUR SDR

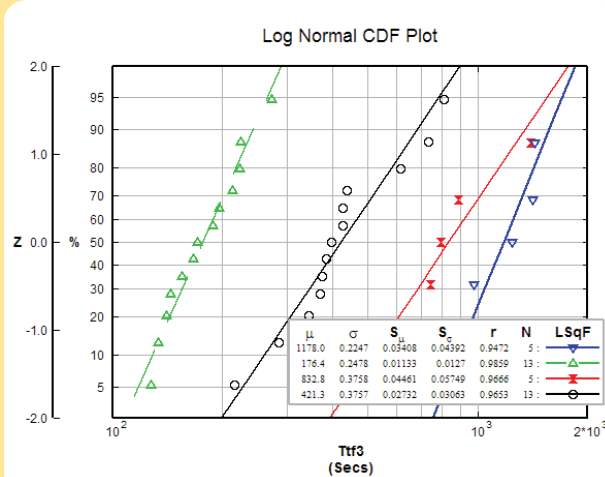
Agilent ASUR SDR is an end-to-end instrument based reliability test cell environment for instrument based solutions, hardware and software. Users have complete access to the JEDEC PDQ-WLR library and instrument control via a standardized TIS library that has same command syntax structure for all supported instruments.

PDQ-WLR, algorithm customization and test development

Users can access the standard PDQ-WLR library through the built-in function or access source code directly for custom development. Users can also develop test plans and algorithms using standard specifications for custom or standard devices using standard hierarchy of wafer, die, test, and probe. Algorithms can also be developed by using graphical development, a programless environment, through IMT.

Data analysis and output formats

All data can be output into flat ASCII files or directly exported to Excel. Users can also choose to configure the built-in data formatters such that algorithms or shell data can be directly imported into corporate databases. All ASUR SDR data is compatible with PDQ-AT and ASUR RDA.



Log normal CDF plot

Upgradeability and compatibility

When the performance of parallel, multi-site testing is required, ASUR SDR customers can upgrade to ASUR PDR with partial or even complete reuse of test instruments.

Compatible with PDQ-WLR on SPECS test plans from 4070 SPECS and algorithm compatibility through common TIS instrument library.



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